CIRCUITS FOR REDUCING LEAKAGE CURRENTS IN PULL-UP AND PULL-DOWN CIRCUITS USING VERY SMALL MOSFET DEVICES

ABSTRACT OF THE DISCLOSURE

A pull-down circuit for pulling a high-impedance node to ground when a pull-down (PD) signal driving the pull-down circuit is Logic 1. The pull-down circuit comprises: 1) a first pull-down N-channel transistor having a drain coupled to the high-impedance node, a gate coupled to the PD signal, and a source coupled to a common node; 2) a second pull-down N-channel transistor having a drain coupled to the common node, a gate coupled to the PD signal, and a source coupled to a ground rail;, wherein the first and second pull-down N-channel transistors are off when the PD signal is Logic 0 and are on when the PD signal is Logic 1; and 3) a gate-biasing circuit driven by the PD signal. The gate-biasing circuit is off when the PD signal is Logic 1 and the gate-biasing circuit applies a Logic 1 bias voltage to the common node when the PD signal is Logic 0. The Logic 1 bias voltage creates a negative Vgs bias on the first pull-down N-channel transistor when the PD signal is Logic 0. An analogous pull-up circuit also is disclosed.